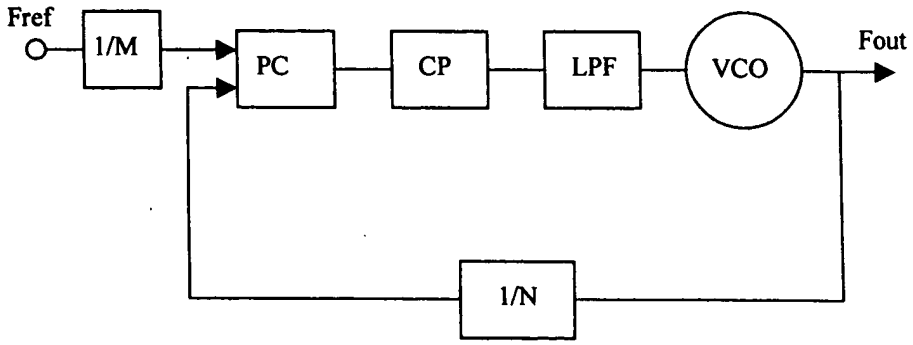

Figure 1. PRIOR ART

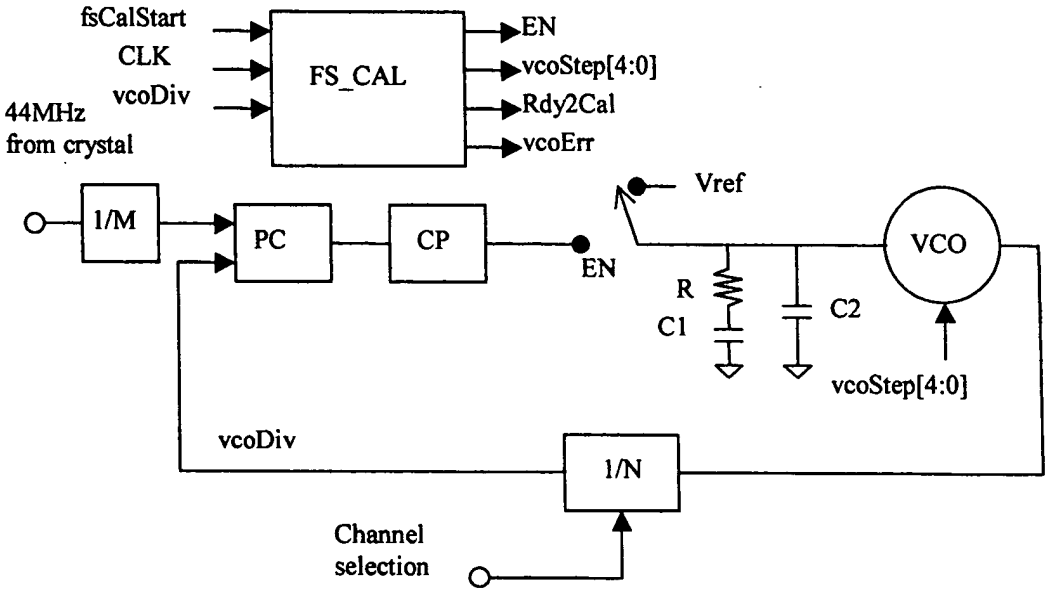

Figure 2.

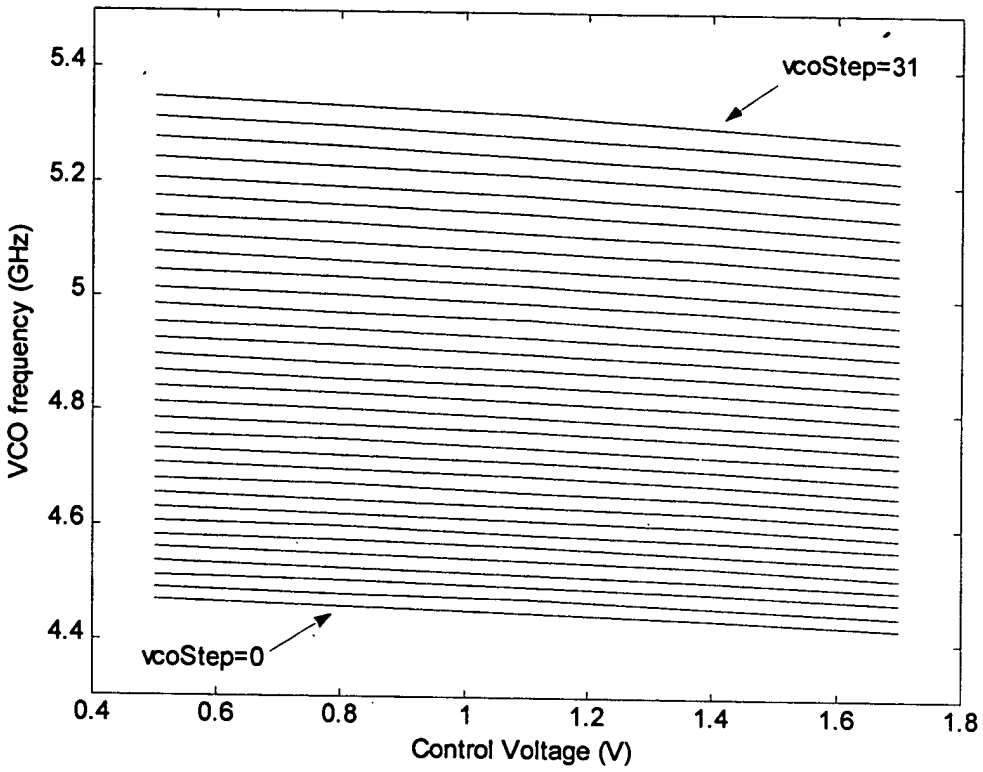
5.4
5.2
5
4.8
4.6
4.4
VCO frequency (GHz)
vcoStep=31
vcoStep=0
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
Control Voltage (V)

Figure 3

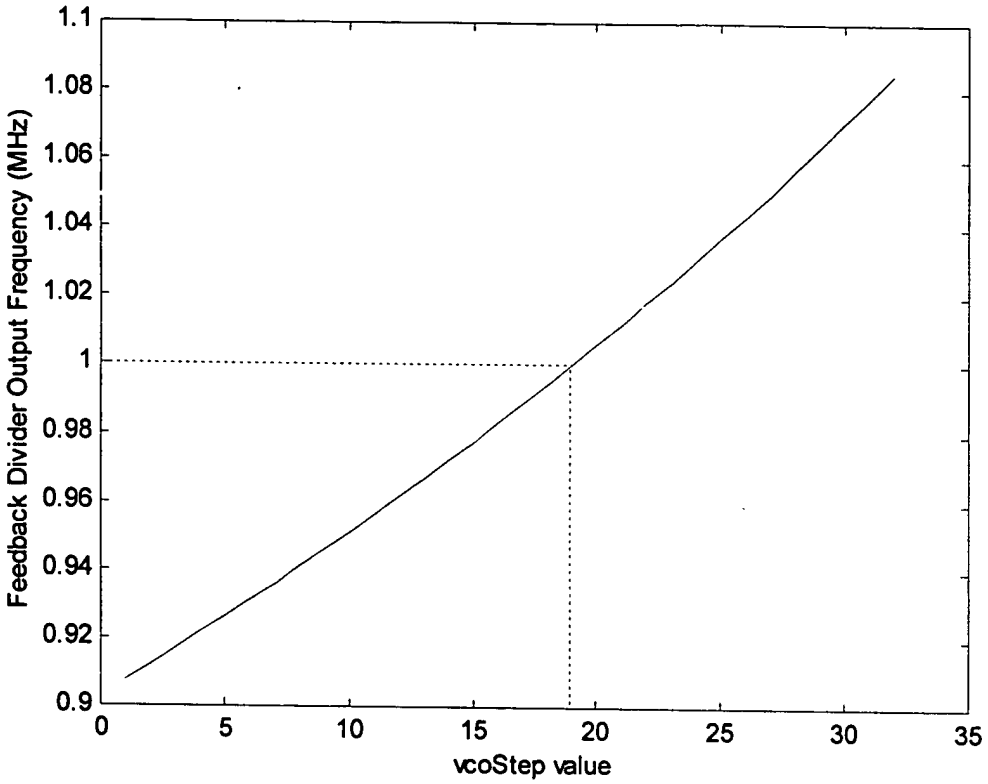

Figure 4.

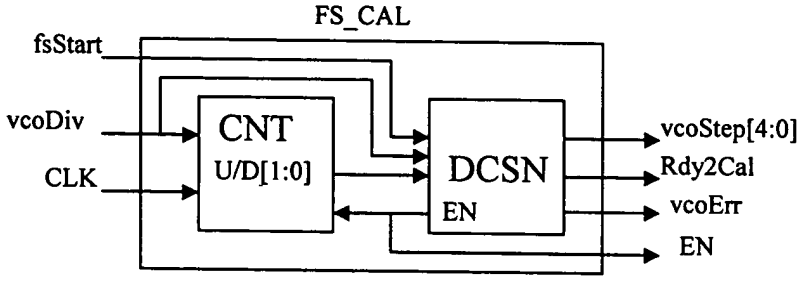

Figure 5.

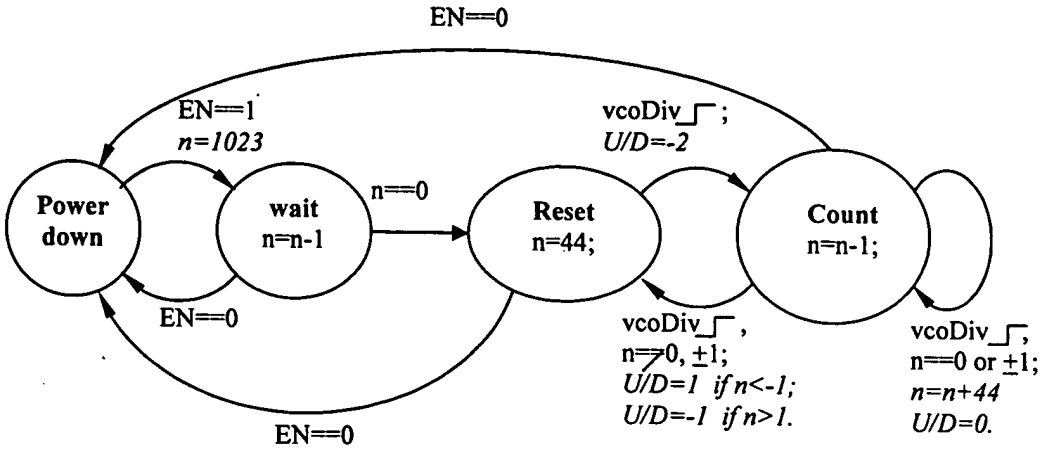

Figure 6.

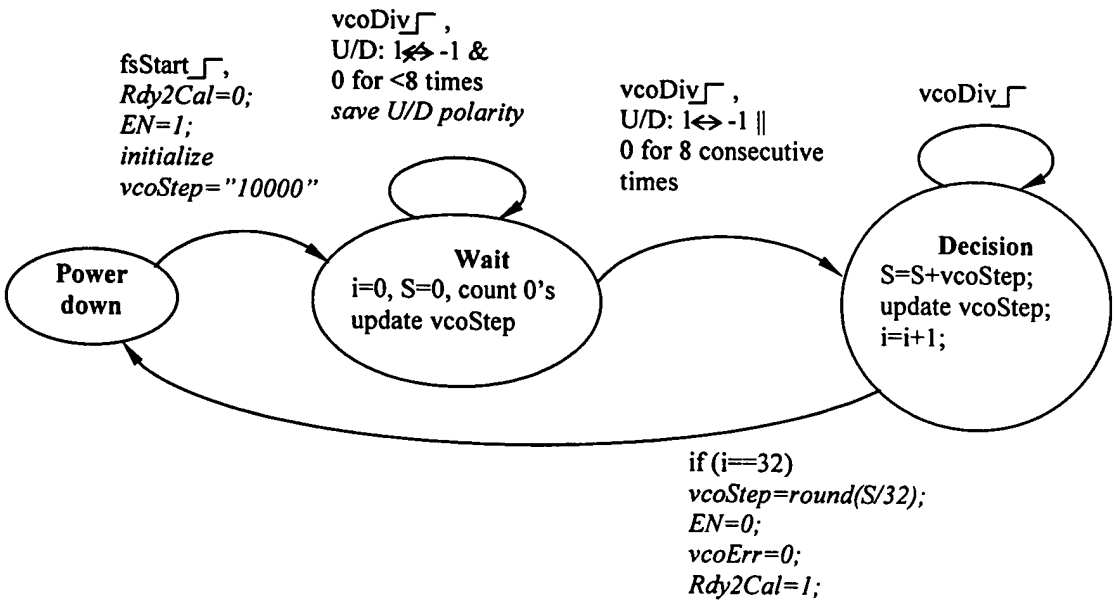

Figure 7.

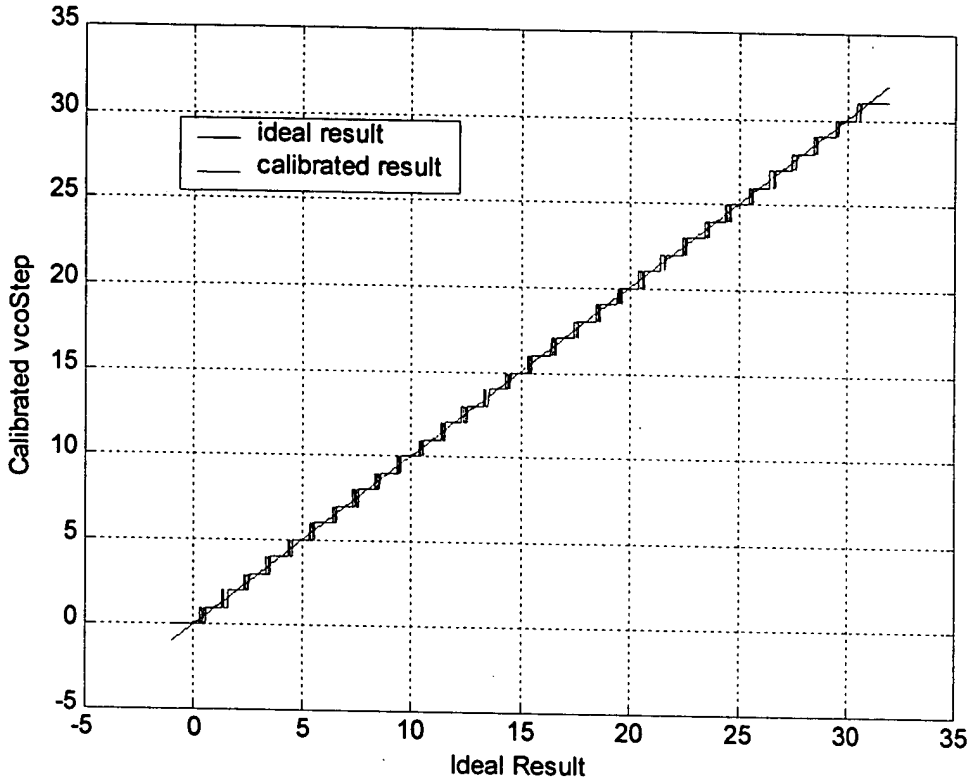
ideal result
calibrated result
Calibrated vcoStep
Ideal Result
35
30
25
20
15
10
5
0
-5
-5
0
5
10
15
20
25
30
35

Figure 8.

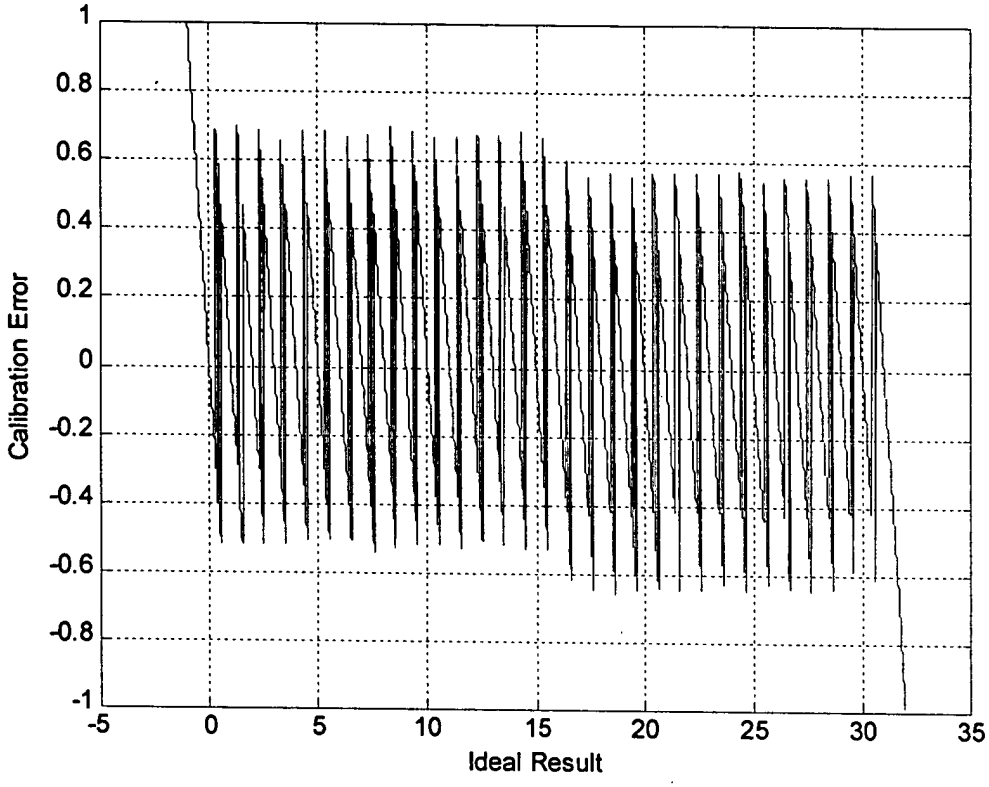
Calibration Error
Ideal Result
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
-5
0
5
10
15
20
25
30
35

Figure 9.

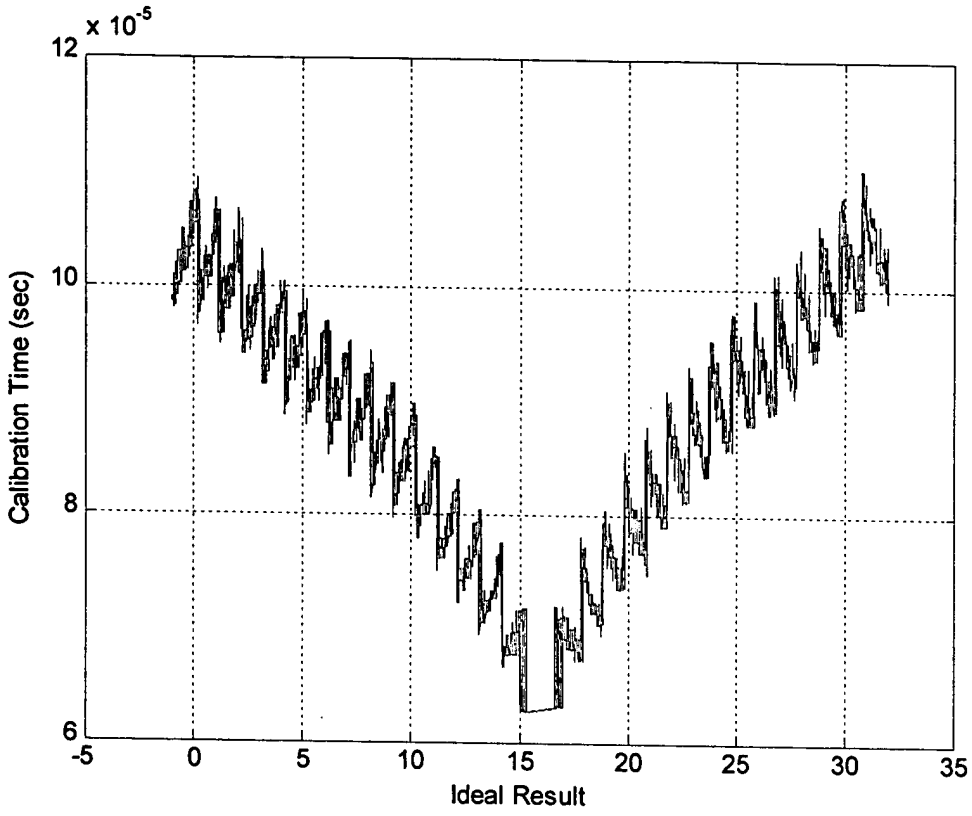

Figure 10.

Pin	I/O	Description
fsStart	I	Rising edge triggers the start of the calibration.
vcoDiv	I	VCO feedback divider output, frequency close to 1MHz, depending on vcoStep[4:0].
CLK	I	44MHz clock from crystal oscillator
vcoStep[4:0]	O	VCO frequency control, "00000": lowest frequency, "11111": highest freqnecy; default: "10000"
Rdy2Cal	O	'1': VCO calibrated; '0': VCO not calibrated; default: '1'
vcoErr	O	'1': VCO calibrated with error; '0': VCO calibrated without error; default: '0'
EN	O	'1': enables CNT, puts PLL into calibration; '0': disables CNT, puts PLL into normal operation; default: '0'
U/D[1:0]	N/A	+1: increment vcoStep; -1: decrement vcoStep; 0: remain unchanged; -2: waiting, remain unchanged

Table 1.